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Is your organization ready for RAMS digitalization? Lessons learned from implementation in an aerospace company

White Paper

Yizhak Bot
bot@bqr.com

SUMMARY & CONCLUSIONS

In this article, we will introduce a new "Engineering & RAMS Digitalization" system (RAMS-D), which will shorten the time needed to perform RAMS analyses and product qualification testing. This method will ensure robust and reliable products with fast Time to Market.

From analyzing the time spent on doing RAMS analyses we found that more than 50% of the time is spent on collecting product data and preparing it for the RAMS analyses. This digitalization system reduces the time spent for creating and standardizing the data.

The digital model includes templates that are plugged into the designer CAD system, IEC standards that standardize the data such as ICD Interface Control Document (IEC-63238-1) and new processes on how to create the data.

This method will help designers from different organizations to generate data in the same format for RAMS analyses.

This new method was implemented during one year in an aerospace company successfully. This article describes the method and its implementation.

1 INTRODUCTION

In order to perform RAMS analyses the RAMS engineer needs to receive the product specifications and product design data. In most cases, he gets many documents, tables and drawings and needs to prepare by himself the product data in the format needed for the RAMS analyses. Below are 2 typical topics:

1. Product hierarchical Block Diagram: The block diagram describes the product from the system level down to assemblies, functions and components. It should include description of each function how it works and the input and output signals. This information is needed for FMECA, testability, safety and RBD. See Fig.1.

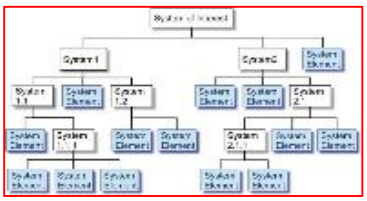

Fig.1: Product hierarchical Block Diagram

2. Component electrical stress: The designer needs to select the correct components rating to comply with a derating criterion. In order to address this requirement, the designer needs to perform a stress analysis for each electronic component. They usually calculate the applied Power, Voltage, Current and Temperature and check if the component operation point is in the Recommended Safe area. If not, a component with a higher rating should be selected. See Fig.2. The stress data is also used for stress derating analysis report and MTBF prediction. Traditionally, the RAMS engineer does not get from the designer the stress data and uses a default value of 50% stress for the MTBF prediction.

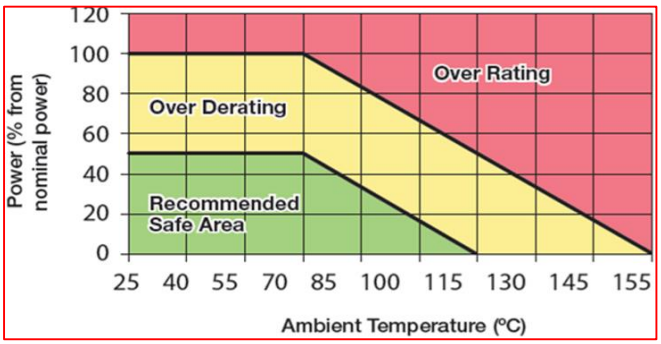

Fig.2: Stress Derating criterion

The new RAMS-D method runs on all the design phases from SDR, PDR, CDR to FDR (System, Preliminary, Critical and Final Design Reviews) and starts with the design CAD tool. Most of the CAD tools support the new method but the engineer does not have a standard to explain the level of documentation he needs to put in the design. In order to bridge the gap, we use a CAD Plug-In tool (Fig.3) which provides a floating window above the circuit schematic. This includes fields and explanations of what the designer should enter and furthermore includes a wizard (Fig4) which teaches step by step the methodology. All this data is stored in a central database that can be used by all RAMS engineers.

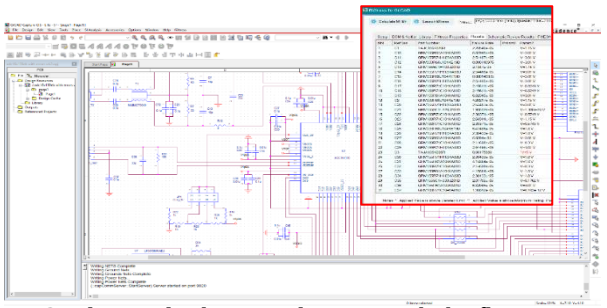

Fig.3: Electrical schematic diagram with the floating window

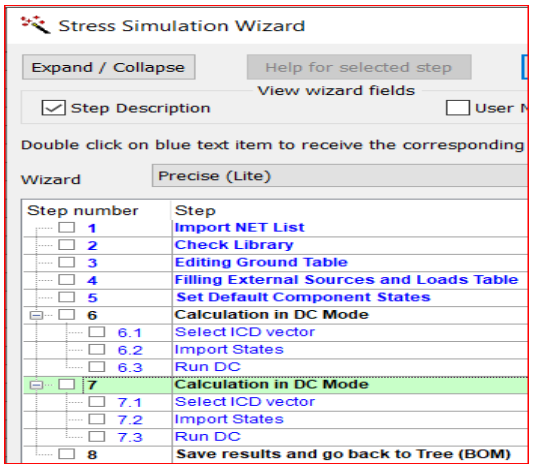

Fig.4: Wizard

2 *PRODUCT HIERARCHICAL BLOCK DIAGRAM*

In this aerospace company, most of the products are made of electronic boards (Fig.5), thus in the traditional way, it is very tedious to break down the product by its functions and is mandatory prior to FMECA. Not only do the designers need to build the block diagram, they also need to split all components into the functional blocks (Fig.6). This task takes 60% of the total FMECA analysis time. With the new method, we reduced this task time to 30 minutes for each board.

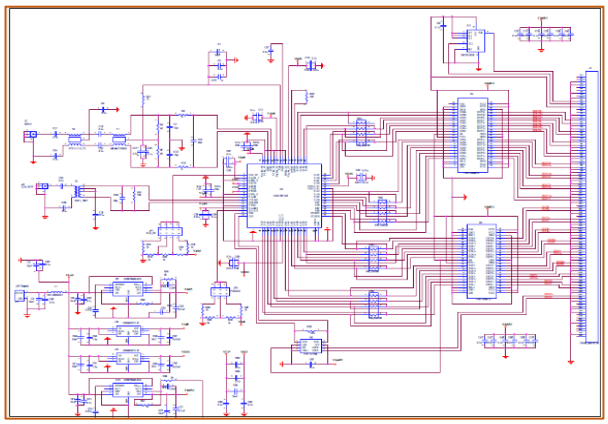

Fig.5: Electronic schematic without function splits

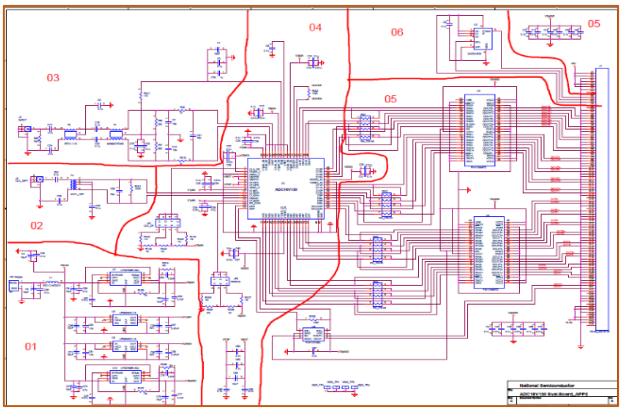

Fig.6: Electronic schematic including function splits

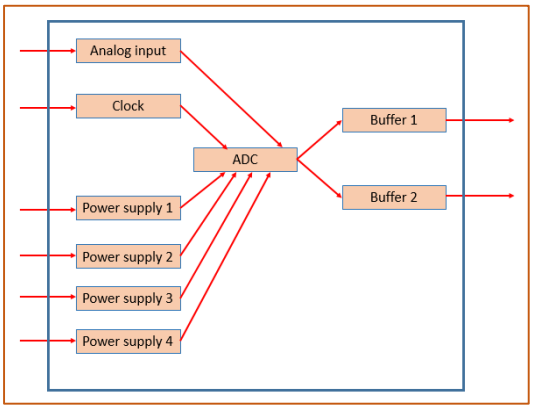

Fig.7: Block diagram

#	Function name	Ref/Des	Description	Failre Rate	Fialure modes
1	Analog input	R1, C1, U1	analog sugnal type 1	0.1	FM1, FM2, FM3, FM4
2	Clock	R2, C2, U2	100Mhz 1 V p2p	0.3	FM1, FM2, FM3, FM4
3	PS1	R3, C3, U3	+5 VDC +/-5%	0.5	FM1, FM2, FM3, FM4
4	PS2	R4, C4, U4	+3.5 VDC +/- 5%	0.5	FM1, FM2, FM3, FM4
5	PS3	R5, C5, U5	+.2.5 VDC +/- 2%	0.5	FM1, FM2, FM3, FM4
6	PS4	R6, C6, U6	+1.8 VDC +/-1%	0.5	FM1, FM2, FM3, FM4
7	ADC	R7, C7, U7	convert analog to digital 16bits	2.1	FM1, FM2, FM3, FM4
8	Buffer 1	R8, C8, U8	output buffer	1.1	FM1, FM2, FM3, FM4
9	Buffer 2	R9, C9, U9	output buffer	1.1	FM1, FM2, FM3, FM4

Fig.8: RAMS data

The traditional way included the following steps and took many days for the RAMS engineer to prepare the data for each board. The steps are:

1. Get the circuit schematic from designer Fig.5.
2. Draw the functional block diagram on the circuit schematic Fig.6.
3. Draw the functional block diagram Fig.7.
4. Dispatch components to functions Fig.8.
5. Calculate failure rate for each component depending on electrical and thermal stress.
6. Accumulate components failure rate to function failure rate Fig.8.
7. Copy the data to FMECA sheets.

With the new method of the CAD Plug-in tool, the circuit designer can easily document the design with valuable information for the RAMS analyses.

The new method, which includes the following steps, takes only 30 minutes for each board.

The steps are:

1. Draws the functional block diagram Fig.7.
2. Describes functions behavior.
3. Runs Stress simulation, derating and MTBF (Para 3.)
4. Prepares data for FMECA.

The main benefit achieved is that the designer can now easily preform design changes and the RAMS engineer will automatically receive the changes to update the RAMS reports.

3 COMPONENT ELECTRICAL STRESS DERATING AND MTBF

This new method provides the designer new tools that help to detect hidden design errors which improve the robustness and reliability of the product. The CAD Plug-In tool performs the following:

- Schematic review to detect hidden design failures (Fig.10)
- Electrical stress simulation
- Derating analysis
- Thermal analysis and
- MTBF Parts Stress predictions.

Part of the digitalization process was to analyze thousands of field failures. By preforming root cause analysis, we detected hundreds of design errors. These design errors were translated into design rules. Thus, when the designer draws a new circuit, the ASR (Automated Schematic Review) detects the hidden design errors, keeping the design clean from mistakes. Afterwards an ASA (Automated Stress Analysis) performs the derating analysis, Fig.9.

While we got into details with the ASR and ASA implementation in the aerospace company, we found that signals between boards are defined differently by each engineer. The signals are also called ICD (Interface Control Document, Para.4) which can generate a big problem in board integrations especially when some of them are developed by ODM (Original Design Manufacturers). By using this new method, we reduce dramatically all qualification and integration tests.

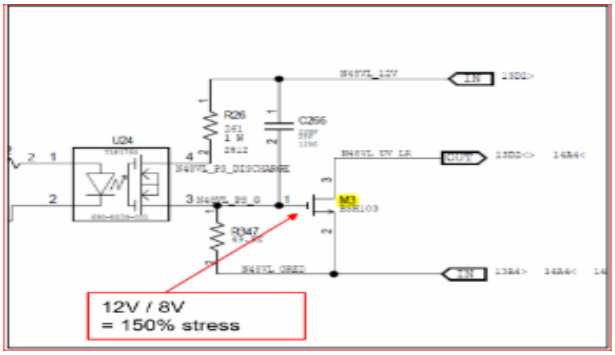

Fig.9: Electrical Over Stress (ESR) problem

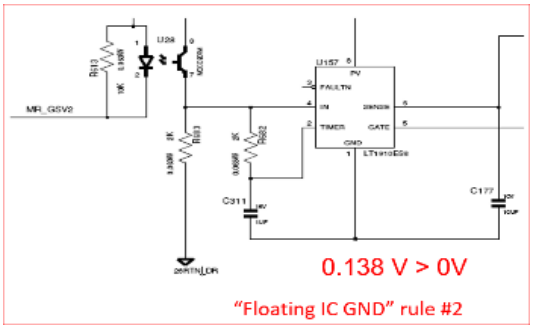

Fig.10: Design error which RAMS techniques cannot detect

4 INTERFACE CONTROL DOCUMENT (ICD)

In our new digitalization model we are using the IEC-63238-1 "Process Management for Avionics – Electronic Design, Part 1: Interface control document (ICD)" which will be released end of 2019.

This IEC standard was developed by BQR, Boeing, Embraer, GE and R-R under the IEC umbrella. The main purpose was to enhance the digitalization process by preparing a standard of signal definitions (Fig.12) that are common across industries thus avoiding misunderstanding and integration issues between assemblies.

In order to simplify the signals and loads definition, the CAD Plug-In module was used. This Plug-in includes a floating window which the designer can select a net (Fig.13) on the design and use the standard signals definitions from the IEC wizard (Fig.11). This simplifies the designer's work and becomes a utility, helping the designer to document the information in the schematic.

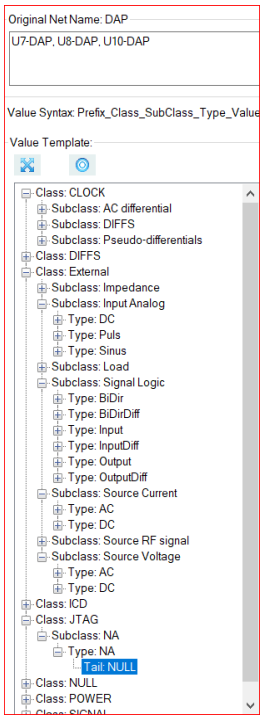

Fig.11: Signals Classes

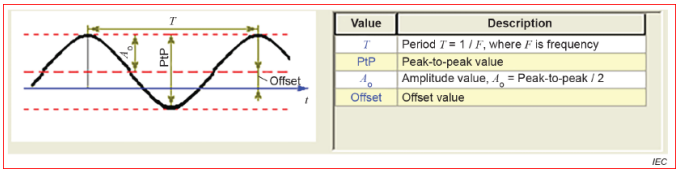

Fig.12: Sample signal definition

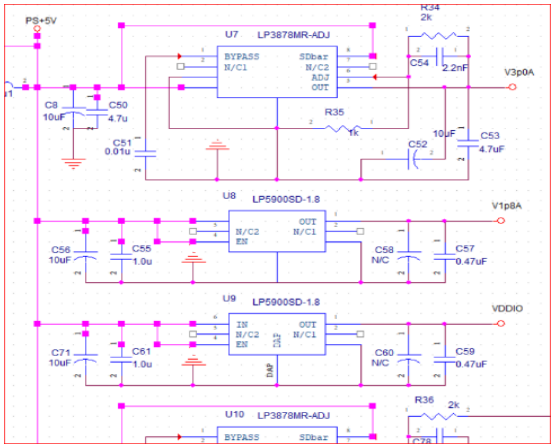

Fig.13 selecting a NET in a schematic

5 SUMMARY

When the aerospace company used the RAMS-D method, they were able to efficiently organize the data and preform the analysis with less iterations. As well, if the design was changed an updated report was quickly generated. In addition, the time it took to perform the following RAMS activities reduced from weeks to a few days:

- Components stress analysis and derating
- Schematic review
- MTBF prediction
- FMEA / FMECA
- Built-In Test analysis
- RBD
- Safety

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BIOGRAPHIES

Yizhak Bot
Rishon-Lezion, Israel

e-mail: bot@bqr.com

Mr. Bot has more than 25 years of experience in Reliability, Availability, Maintainability and Safety (RAMS) and Integrated Logistic Support (ILS). He was the RAM/ILS manager of many defense and commercial projects worth more than 25 Billion US Dollars. He has written articles for leading magazines, conducted seminars and gave lectures worldwide. He is also the inventor of fiXtress, CARE and apmOptimizer technologies.

From 1989 he is the president of BQR, a leading consulting and software-developing firm. In previous employments, he was a Reliability and ILS Engineer, freelance adviser (1984-1989), Tadiran Telecommunication (1980-1984) and Israel Defense Force (IDF) (1970-1980).